AMENDMENTS TO THE CLAIMS

Claims 1-66 (canceled).

67. (Currently amended) A method of calibrating a data path of a digital circuit, the method comprising the acts of:

positioning a clock transition of a clock signal at one edge of a data eye of a bit of data received on said data path; and

relocating said clock transition to approximately a center of said data eye based on said one edge.

68. (Previously presented) The method of claim 67, wherein said act of positioning comprises:

adjusting relative timing of said bit of data with respect to said clock transition.

69. (Previously presented) The method of claim 67, further comprising:

clocking said bit of data on said data path into said digital circuit.

70. (Previously presented) The method of claim 67, wherein said act of relocating comprises:

adjusting relative timing of the bit of data with respect to said clock signal by a predetermined amount which is approximately equal to one-half of a width of said data eye.

71. (Previously presented) The method of claim 70, wherein said act of adjusting comprises:

delaying said bit of data by said predetermined amount.

72. (Previously presented) The method of claim 70, wherein said act of adjusting comprises:

advancing said bit of data by said predetermined amount.

73. (Previously presented) A system for calibrating a data path of a digital circuit, the system comprising:

a logic circuit for positioning a clock transition of a clock signal at one edge of a data eye of a bit of data received on said data path;

said logic circuit also being configured to relocate said clock transition to approximately a center of said data eye based on said one edge.

74. (Previously presented) The system of claim 73, wherein said logic circuit is configured to adjust relative timing of said bit of data with respect to said clock transition.

75. (Previously presented) The system of claim 73, further comprising:

a latch circuit for clocking said bit of data on said data path into said digital circuit using said clock signal.

76. (Previously presented) The system of claim 73, wherein said logic circuit is configured to adjust relative timing of the bit of data with respect to said clock signal

by a predetermined amount which is approximately equal to one-half of a width of said data eye.

77. (Previously presented) The system of claim 76, wherein said logic circuit is configured to delay said bit of data by said predetermined amount.

78. (Previously presented) The system of claim 76, wherein said logic circuit is configured to advance said bit of data by said predetermined amount.

79. (Previously presented) An integrated circuit semiconductor device comprising a system for calibrating a data path of a digital circuit, the system comprising:

a logic circuit for positioning a clock transition of a clock signal at one edge of a data eye of a bit of data received on said data path;

said logic circuit also being configured to relocate said clock transition to approximately a center of said data eye based on said one edge.

80. (Previously presented) The device of claim 79, wherein said logic circuit is configured to adjust relative timing of said bit of data with respect to said clock transition.

81. (Previously presented) The device of claim 79, wherein said system further comprises:

a latch circuit for clocking said bit of data on said data path into said digital circuit using said clock signal.

82. (Previously presented) The device of claim 79, wherein said logic circuit is configured to adjust relative timing of the bit of data with respect to said clock signal by a predetermined amount which is approximately equal to one-half of a width of said data eye.

83. (Previously presented) The device of claim 82, wherein said logic circuit is configured to delay said bit of data by said predetermined amount.

84. (Previously presented) The device of claim 82, wherein said logic circuit is configured to advance said bit of data by said predetermined amount.

85. (Previously presented) The device of claim 82, wherein said system further comprises:

a receiver for receiving said bit of data;

a storage device coupled to said receiver for temporarily storing a predetermined number of bits of said data; and

an examining device coupled to said storage device for examining said predetermined number of bits of data for a predetermined bit pattern.

86. (Previously presented) A processor system, comprising:

a processor; and

a dynamic random access memory (DRAM) coupled to said processor, at least one of said processor and memory having a system for calibrating a data path of a digital circuit, said system for calibrating comprising:

a logic circuit for positioning a clock transition of a clock signal at one edge of a data eye of a bit of data received on said data path;

said logic circuit also being configured to relocate said clock transition to approximately a center of said data eye based on said one edge.

87. (Previously presented) The processor system of claim 86, wherein said logic circuit is configured to adjust relative timing of said bit of data with respect to said clock transition.

88. (Previously presented) The processor system of claim 86, wherein said system for calibrating further comprises:

a latch circuit for clocking said bit of data on said data path into said digital circuit using said clock signal.

89. (Previously presented) The processor system of claim 86, wherein said logic circuit is configured to adjust relative timing of the bit of data with respect to said clock signal by a predetermined amount which is approximately equal to one-half of a width of said data eye.

90. (Previously presented) The processor system of claim 89, wherein said logic circuit is configured to delay said bit of data by said predetermined amount.

91. (Previously presented) The processor system of claim 89, wherein said logic circuit is configured to advance said bit of data by said predetermined amount.

92. (Previously presented) The processor system of claim 89, wherein said system for calibrating further comprises:

a receiver for receiving said bit of data,

a storage device coupled to said receiver for temporarily storing a predetermined number of bits of said data; and

an examining device coupled to said storage device for examining said predetermined number of bits of data for a predetermined bit pattern.